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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/550,405	04/14/2000	Eiji IO	APM-01301	8514

26339 7590 02/13/2004

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/550,405	IO, EIJI	
	Examiner	Art Unit	
	ori nadav	2811	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d f r R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-11 and 20-23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of heavily doped second source and drain regions ... aligned with at least one sidewall, with said first drain and source diffusion layers surrounding said second drain and source diffusion layers on at least a bottom and a lateral side, as recited in claims 1 and 6, are unclear as to how the phrase "with said first drain and source diffusion layers surrounding said second drain and source diffusion layers on at least a bottom and a lateral side" is related to the previous phrase.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 3-6, 9-11, 20 and 22, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez (5,439,835) in view of Cheng et al. (5,545,575).

Regarding claims 1, 3, 5, 6, 9 and 11, Gonzalez teaches in figure 9 and related text a semiconductor device comprising a memory cell formed on a semiconductor substrate 12, an insulating layer 13 defining device regions, a gate region 16, heavily doped second source and drain regions 23 (figure 2) around the gate electrode and aligned with at least one sidewall, with said first drain and source diffusion layers surrounding said second drain and source diffusion layers on at least a bottom and a lateral side,

said at least one sidewall 41 (figure 4) covering the gate electrode and having connected thereto a sidewall offset extending outwardly of the gate electrode along a horizontal surface of the substrate above only one of the second source and drain regions and along a lateral surface of a gate oxide by an amount that is greater than a thickness of the sidewall,

low resistive wiring layers 92, 51 (figure 5) formed at surfaces of the source and drain layers being located outwardly beyond a peripheral edge of the sidewall offset,

and said heavily doped second source and drain region layers extending below the sidewall offset but spaced outwardly away from the edge of the gate electrode in a direction along said horizontal surface of the semiconductor substrate.

Gonzalez does not teach lightly doped first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and a

lateral side and extending towards the gate electrode beyond an edge of the sidewall offset.

Cheng et al. teach in figure 7 lightly doped first drain and source diffusion layers 43, 44 surrounding second drain and source diffusion layers 57, 58 on at least a bottom and a lateral side and extending towards the gate electrode beyond an edge of the sidewall offset.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides, as taught by Cheng et al., wherein the first drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset, in Gonzalez's device, in order to improve the device characteristics by forming LDD regions in the device, and in order adjust and optimize the device characteristics by extending the first drain and source diffusion layers towards the gate electrode beyond an edge of the sidewall offset.

Regarding claims 4 and 10, Cheng et al. teach in figure 7 second diffusion layers 43, 44 of lower impurity concentration than that of the source and drain regions 57, 58 (column 4, lines 24-26 and column 6, lines 2-4) formed below the source and drain regions.

Regarding claim 6, Cheng et al. teach in figure 7 silicide wiring layers 64 formed at surfaces and in the source and drain layers located outwardly beyond a peripheral edge

of the sidewall offset. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form silicide wiring layers at surfaces and in the source and drain layers located outwardly beyond a peripheral edge of the sidewall offset in Gonzalez's device in order to reduce the contact resistance of the device.

Regarding claims 20 and 22 Gonzalez teaches in figure 9 only one sidewall offset.

4. Claim 7, insofar as in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez and Cheng et al., as applied to claim 6 above, and further in view of Kunishima et al. (5,316,977).
Gonzalez and Cheng et al. teach substantially the entire claimed structure, as applied to claim 1 above, except a silicide layer comprising titanium silicide.
Kunishima et al. teach in figure 5C a silicide layer 21 comprising titanium silicide.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a titanium silicide in Gonzalez and Cheng et al.'s device, because titanium silicide is a conventional silicide material, of which official notice is taken.

5. Claims 1-4, 6, 8-10, 21 and 23, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al.
Cheng et al. teach in figure 15 a semiconductor device comprising a semiconductor substrate 11, an insulating layer 19 defining device regions, a gate region 28 and the

insulating layer defining lightly doped first drain or source diffusion layers 77', 78', heavily doped second source and drain regions 82, 84 around the gate electrode and aligned with at least one sidewall, with the first drain and source diffusion layers 77', 78' surrounding the second drain or source diffusion layers 82, 84 on at least a bottom and a lateral side,

at least one sidewall 66 covering the gate electrode and having connected thereto a sidewall offset extending outwardly of the gate electrode along a horizontal surface of the substrate in both regions above the second source and drain regions and along a lateral surface of a gate oxide by an amount that is greater than a thickness of the sidewall,

silicide wiring layers 64 formed at surfaces of the source and drain layers being located outwardly beyond a peripheral edge of the sidewall offset,

and said heavily doped second source and drain region layers extending below the sidewall offset but spaced outwardly away from the edge of the gate electrode in a direction along said horizontal surface of the semiconductor substrate.

Cheng et al. do not teach in the embodiment of figure 15 first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and a lateral side and extending towards the gate electrode beyond an edge of the sidewall offset.

Cheng et al. teach in the embodiment of figure 7 first drain and source diffusion layers 43, 44 surrounding second drain and source diffusion layers 57, 58 on at least a bottom

and a lateral side, wherein the first drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form first drain and source diffusion layers surrounding the second drain and source diffusion layers on at least a bottom and four lateral sides wherein the first drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset, in Cheng et al.'s device, in order to improve the device characteristics by forming LDD regions in the device, and in order adjust and optimize the device characteristics by extending the first drain and source diffusion layers towards the gate electrode beyond an edge of the sidewall offset.

Regarding claims 21 and 23, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to cover entirely the gate electrode of Cheng et al.'s device with the sidewall in order to provide better protection for the gate in an application which does not require external connection to the gate.

6. Claims 5, 7, 11, 21 and 23, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al., as applied to claims 1 and 6 above, and further in view of Kunishima et al.

Cheng et al. teach substantially the entire claimed structure, as applied to claims 1 and 6 above, except a silicide layer comprising titanium silicide.

Kunishima et al. teach in figure 5C a silicide layer 21 comprising titanium silicide.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a titanium silicide in Cheng et al.'s device, because titanium silicide is a conventional silicide material, of which official notice may be taken.

Regarding claims 5 and 11, Kunishima et al. teach using the semiconductor device as a CMOS device, and it is well known in the art that CMOS devices are used as memory devices. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Cheng et al.'s device as a memory device, because the intended use of a device depends on the requirements of the application in hand. Note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claims 21 and 23, Kunishima et al. teach in figure 5C a sidewall entirely covering the gate electrode. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to cover entirely the gate electrode of Cheng et al.'s device with the sidewall in order to provide better protection for the gate in an application which does not require external connection to the gate.

Respons to Arguments

7. Applicant argues on page 9 that Gonzalez does not teach heavily doped second source and drain regions being formed aligned with at least one sidewall.

Figure 9 of Gonzalez depicts heavily doped second source and drain regions being aligned with at least one sidewall. Therefore, Gonzalez teaches heavily doped second source and drain regions being aligned with at least one sidewall, as claimed.

Applicant argues that prior art does not teach heavily doped second source and drain region layers extending below the sidewall offset but spaced outwardly away from the edge of the gate electrode in a direction along said horizontal surface of the semiconductor substrate.

Gonzalez teaches in figure 9 multiple heavily doped second source and drain region layers formed to the right and to the left of gate electrodes 16, and extending below the sidewall offset but spaced outwardly away from the edge of the gate electrode in a direction along said horizontal surface of the semiconductor substrate, as claimed. Regarding the Cheng et al. reference, although Cheng et al. teach heavily doped second source and drain region layers overlapping vertically with the gate electrode, the heavily doped second source and drain region layers still extend below the sidewall offset and spaced outwardly away from the edge of the gate electrode in a direction along said horizontal surface of the semiconductor substrate, as claimed.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related t Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
February 7, 2004

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800